LISTING OF CLAIMS:

1-5. (Cancelled)

6. (Currently Amended) ~~The method of claim 1, further comprising:~~

A method for generating pseudo random test patterns for simulating a hardware model comprising:

generating a driver model having a plurality of states, wherein each state indicates whether to drive an interface of the hardware model;

initiating a random walk through the driver model to generate a driver test pattern;

controlling simulation of the hardware model using the driver test pattern;

generating a command model having a plurality of states, wherein each state indicates a command to send across an interface of the hardware model;

initiating a random walk through the command model to generate a command test pattern; and

controlling simulation of the hardware model using the command test pattern.

7. (Original) The method of claim 6, wherein the step of generating a command model comprises:

creating at least one command subgraph having a plurality of command states; and

connecting the at least one command subgraph to form the command model.

8. (Original) The method of claim 7, wherein each command subgraph comprise a Markov chain.

9. (Original) The method of claim 7, wherein each state has a probability of transitioning to at least one other state.

10-14. (Cancelled)

15. (Currently Amended) ~~The apparatus of claim 10, further comprising:~~

An apparatus for generating pseudo random test patterns for simulating a hardware model comprising:

generation means for generating a driver model having a plurality of states, wherein each state indicates whether to drive an interface of the hardware model;

initiation means for initiating a random walk through the driver model to generate a driver test pattern;

control means for controlling simulation of the hardware model using the driver test pattern;

means for generating a command model having a plurality of states, wherein each state indicates a command to send across an interface of the hardware model;

means for initiating a random walk through the command model to generate a command test pattern; and

means for controlling simulation of the hardware model using the command test pattern.

16. (Original) The apparatus of claim 15, wherein the means for generating a command model comprises:

means for creating at least one command subgraph having a plurality of command states; and

means for connecting the at least one command subgraph to form the command model.

17. (Original) The apparatus of claim 16, wherein each command subgraph comprises a Markov chain.

18. (Original) The apparatus of claim 16, wherein each state has a probability of transitioning to at least one other state.

19. (Cancelled)

20. (Currently Amended) ~~The computer program product of claim 19, further comprising:~~

A computer program product, in a computer readable medium, for generating pseudo random test patterns for simulating a hardware model comprising:

instructions for generating a driver model having a plurality of states, wherein each state indicates whether to drive an interface of the hardware model;

instructions for initiating a random walk through the driver model to generate a driver test pattern;

instructions for controlling simulation of the hardware model using the driver test pattern;

instructions for generating a command model having a plurality of states, wherein each state indicates a command to send across an interface of the hardware model;

instructions for initiating a random walk through the command model to generate a command test pattern; and

instructions for controlling simulation of the hardware model using the command test pattern.